

Claims

- [c1] A method of forming a semiconductor device, comprising:
- providing a semiconductor structure comprising a silicon substrate and a gate structure formed on the silicon substrate, said gate structure further comprising a gate contact and a gate insulator;
 - selectively forming etched-away areas in the substrate to expose sides of a channel region under the gate structure;
 - disposing a thin, highly-doped layer of a silicidation stop material within the etched-away areas;
 - disposing a silicon fill within the etched-away areas over the silicidation stop material to; and
 - performing silicidation to form silicide in the silicon fill, thereby forming source/drain silicide regions.
- [c2] A method according to claim 1, wherein the silicidation step is performed at a temperature above a silicidation threshold temperature for the silicide in silicon, but below a silicidation threshold temperature for the silicide in the silicidation stop material.
- [c3] A method according to claim 2, wherein the silicidation

stop material is SiGe.

- [c4] A method according to claim 3, wherein the silicide is CoSi_2 (cobalt silicide).
- [c5] A method according to claim 4, wherein the silicidation step is performed at a temperature above a silicidation threshold temperature CoSi_2 formatting in silicon (Si) and below a silicidation threshold temperature for CoSi_2 formation in SiGe.
- [c6] A method according to claim 4, wherein the silicidation step is performed at a temperature above 640°C and below 780°C.
- [c7] A method according to claim 1, wherein the silicidation stop material is in-situ doped.
- [c8] A method according to claim 1, wherein the thickness of silicidation-stop extensions is less than 50% of the thickness of the silicide lateral extensions.
- [c9] A method according to claim 8, wherein the thickness of the silicidation-stop extensions is greater than a minimum thickness defined by the depletion thickness for an active dopant concentration in the silicidation stop material.
- [c10] A method according to claim 9, wherein the active

dopant concentration is greater than 10^{19} atoms/cm³.

- [c11] A method according to claim 9, wherein the minimum thickness is 10Å.
- [c12] A method according to claim 1, wherein the semiconductor structure is an inchoate n-channel MOSFET.
- [c13] A method according to claim 1, wherein the semiconductor structure is an inchoate p-channel MOSFET.
- [c14] A method according to claim 1, wherein the semiconductor structure is part of an inchoate CMOS device.
- [c15] A semiconductor device having silicide-stop extensions, comprising:
 - a semiconductor structure comprising a substrate and a gate structure formed on the substrate, said gate structure further comprising a gate insulator and a gate electrode;
 - silicide source/drain regions; and
 - silicide-stop extensions composed of a highly-doped silicidation-stop material interposed between the silicide source/drain regions and the substrate such that the source/drain silicide regions are separated thereby from a channel region underlying the gate structure and the substrate.

- [c16] A semiconductor device according to claim 15, wherein the silicidation stop material is SiGe.
- [c17] A semiconductor device according to claim 16, wherein the source/drain silicide regions are CoSi_2 (cobalt silicide).
- [c18] A semiconductor device according to claim 15, wherein silicide-stop extension thickness is less than 50% of source/drain silicide region thickness.
- [c19] A semiconductor device according to claim 18, wherein the thickness of the silicidation-stop extensions is greater than a minimum thickness defined by the depletion thickness for an active dopant concentration in the silicidation stop material.
- [c20] A method according to claim 18, wherein the active dopant concentration is greater than 10^{19} atoms/cm³.
- [c21] A method according to claim 18, wherein the minimum thickness is 15Å.
- [c22] A semiconductor device according to claim 15, wherein the semiconductor structure is an inchoate n-channel MOSFET.
- [c23] A semiconductor device according to claim 15, wherein the semiconductor structure is an inchoate p-channel

MOSFET.

- [c24] A semiconductor device according to claim 15, wherein the semiconductor structure is part of an inchoate CMOS device.
- [c25] A semiconductor device, comprising:
a semiconductor structure comprising a substrate and a gate structure formed on the substrate, said gate structure further comprising a gate insulator and a gate electrode;
silicide source/drain regions formed of CoSi_2 (cobalt silicide);
highly-doped SiGe silicide-stop extensions interposed between the silicide source/drain regions and the substrate such that the source/drain silicide regions are separated thereby from a channel region underlying the gate structure and the substrate;
wherein:
SiGe silicide-stop extension thickness is less than 50% of silicide source/drain region thickness; and
SiGe silicide-stop extension thickness is greater than a minimum defined by a depletion thickness for a level of active dopant concentration in the silicide-stop extensions.